International Journal of Scientific Engineering and Technology
Volume No.5 Issue No.10, pp: 471-476

ISSN:2277-1581
01 October 2016

Testing of CMOS OTA Using Combined Oscillation and I_{DDQ} Test Methodology

Maninder Kaur* , Jasdeep Kaur
*Guru Tegh Bahadur Institute of Technology, affiliated to Guru Gobind Singh Indraprastha University, New Delhi, India
Indira Gandhi Delhi Technical University for Women Kashmere Gate, New Delhi, India
Email: mindersaini82@gmail.com

Abstract: In this paper, a technique integrating Oscillation and I_{DDQ} based test methodology for two stage CMOS operational transconductance amplifier is presented. The approach is attractive for its simplicity, robustness of oscillation based test technique that needs no test signal generation and combines it with quiescent supply current testing which utilized the built in current sensor to monitor quiescent current changes without performance degradation of the circuit under test. Both short and open faults are detected by this test methodology. Simulation results for two stage operational transconductance amplifier using a 0.18µm n-well CMOS technology show that the proposed combined test strategy has 100% fault coverage and capability of built-in-self test implementation. It can also be used as generalized test structure for other CMOS analog and mixed-signal integrated circuits.

Keywords: Operational transconductance amplifier (OTA), Circuit under test (CUT), Monte-Carlo simulation, faults, OTM, BICS.

I. Introduction

Testing of mixed or analog integrated circuits is considered as one of the most important problem in VLSI circuits using CMOS technology [1]. Analog circuit have been tested for critical specification such as linearity, common-mode rejection ratio, signal to noise ratio, slew rate, ac gain , common-mode rejection ratio, that result in long testing time, poor fault coverage, high cost [2]. Reducing test time by optimizing the functional test set while achieving the desired fault coverage has also been studied. However, the technique needs a reasonable large number of sample circuit for collecting the test data. Hence, we need to explore and investigate some cost effective test method without any additional signal generation circuit [3].

In this paper, we present low cost test approach to improve the fault diagnosis and testability of typical two-stage CMOS operational transconductance amplifier based on oscillation test methodology and is also combined with I_{DDQ} testing technique to provide a fault confirmation. The proposed test methodology is simple and provides good fault coverage with small circuit modification.OTM is a vector-less technique as it does not require any test signal generation [4]. The process comprises of dividing the circuit under test into small functional blocks like amplifier, comparator, filter etc and each block is transformed to a circuit which oscillates. The oscillation frequency of the CUT is compared with nominal frequency of fault free circuit and difference between oscillation frequency and nominal frequency indicates the presence of fault. Monte Carlo analysis is used to determine the tolerance band of the oscillation frequency taking into account the nominal tolerance of all CUT components. Fault-injection technique is used in the testing procedure to enhance the testability of CUT. The approach is attractive for its simplicity and robustness [5].

On the other side, I_{DDQ} test is a cost effective method for detecting the faults which are undetected by the conventional test method. I_{DDQ} testing is a current-based test method that does not require propagation of a fault effect to an observed output. It requires only exercising the fault circuit and then calculating the current from power supply. The fault is observed by the measurement of current which exceed some threshold limit [6]. The circuit draws a very low current (µA) in the quiescent state but for the certain input state due to presence of faults, this current may raise to an abnormal level. A simple built-in current sensor (BICS), which introduces insignificant performance degradation of CUT is presented to detect short (Bridging) and open faults. Two-stage CMOS operational transconductance amplifier is used as circuit under test which operates at ±1.5V. OTA is voltage controlled current source which produces an output current with differential input voltage. It is voltage controlled current source. OTA constitute as a major building block in the analog circuits such as ADC, DAC, four-quadrant multipliers, mixers, modulators and continuous-time filters etc [7]. Schematic diagram of two-stage CMOS OTA used for simulation is shown in fig1.

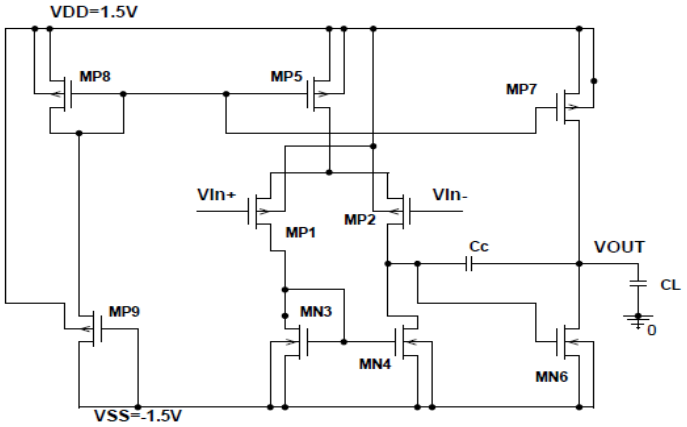


Fig.1: Low voltage Two-stage CMOS OTA (CUT)

ISSN:2277-1581
01 October 2016

The format of this paper is as follows; oscillation test strategy and CUT into oscillator conversion are discussed in section II and section III respectively. Section IV introduces IDDQ test methodology whereas section V describes the design consideration for BICS. Section VI and section VII describe the analog fault modelling and Monte-Carlo simulation respectively. Test simulation results are given in Section VIII and Section IX contains conclusions.

II. **Oscillation Test Strategy Description**

The oscillation based testing is the robust, simple and vector-less test technique without need of test signal generation. The OTM is based on first partitioning the mixed and analog signal integrated circuit into functional building blocks such as amplifier, comparator, filter, and data converter. Each block is transformed into an oscillating circuit by the addition of external circuitry in their feedback path [8]. The test is performed by evaluating the oscillation frequency (fosc) of CUT. Oscillation frequency of CUT is compared with the nominal oscillation frequency of the fault free circuit. If the oscillation frequency of CUT is equal to the nominal frequency range, the CUT is accepted to be fault-free. When a reasonable deviation of the oscillation frequency of CUT from its tolerance band occurs, the fault is detectable. Monte-Carlo simulation is used to determine the nominal frequency range of CUT while taking into account the tolerance of significant technology and design parameters [9, 10].

The oscillator design must be chosen so as to ensure the maximum possible CUT elements contribution in describing the oscillation frequency.

III. **Conversion of CUT into Oscillator**

The OTA (CUT) is transformed to oscillator circuit by adding circuit in the feedback loop whose oscillation frequency can be defined as function of the CUT components or its important parameters. The oscillations condition (Barkhausen criterion) of CUT as an oscillator is maintained in its transfer function with no attenuation and no phase shift by adjusting the feedback loop elements [11]. The transfer function of the oscillator is given by equation (1):

$$f_{osc} = \frac{f_{CUT}}{1 - f_{CUT} f_H} \tag{1}$$

Where f_{CUT} and f_H represents the transfer function of the CUT and feedback element respectively. The oscillation frequency f_{osc} and oscillation condition are obtained from equations (2), (3) and (4).

$$f_{CUT}(j\omega) f_H(j\omega) = 1 \tag{2}$$

Or equivalently:

$$Re(f_{CUT}(j\omega) f_H(j\omega)) = 1 \tag{3}$$

$$\mathrm{Im}(f_{CUT}(j\omega) f_H(j\omega)) = 1 \tag{4}$$

This condition is Barkhausen criterion which defines that the signal must transverse the loop with no attenuation and no phase shift at the oscillation frequency [12].

In the present work, Wien bridge network is used to convert CUT is converted into oscillator as shown in fig 2. The component values that are used here are $R_1 = R_3 = 10K\Omega$, $R_2 = 3\ K\Omega$, $R_4 = 1K\Omega$, $C_3 = C_1 = 16nF$ for simulation to achieve self-sustained oscillation [13].

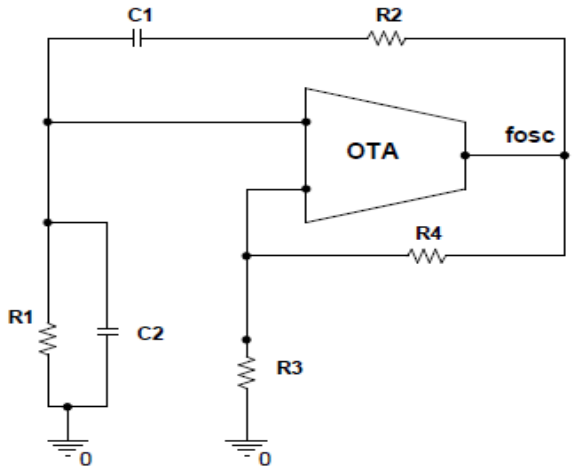


Fig. 2: Block diagram of CUT as an oscillator

Natural oscillation frequency is determined by the Fast Fourier Transform (FFT) analysis of oscillatory circuit.

IV. **I_{DDQ} Testing**

I_{DDQ} testing based on calculating the steady state power supply current. It comprises of observing the quiescent current on supply voltage allowing a precise coverage of physical defects in the CUT [14]. Under the fault conditions, the normal values of quiescent current may be increased, decreased or generally distorted. Thus, fault detection can be accomplished by monitoring the quiescent current fluctuations using a current sensing circuit. Any current above the quiescent current would indicate the presence of physical defects in the circuit [15]. A built-in current sensor (BICS) has been used to monitor the changes in the quiescent current in the power supply rails that introduces insignificant performance degradation of CUT as shown in fig 3.

ISSN:2277-1581
01 October 2016

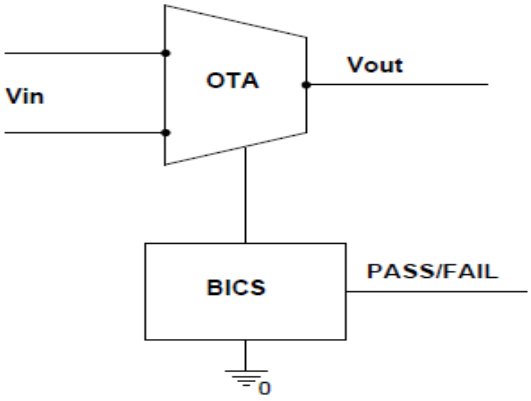


Fig. 3: Block Diagram of I_{DDQ} testing

V. **Design Consideration of BICS**

In I_{DDQ} testing, the BICS embedded in series with VDD or GND lines of the CUT checks whether the quiescent current is below or above a threshold level [28]. The existence of fault without performance degradation of CUT is indicated by proposed BICS. For effective use of internal testing, the BICS must minimize the effect of capacitance and voltage drop and achieve minimum disturbances in the CUT.

In the present work, a simple design of a built-in current sensor is presented to detect bridging faults and open faults in CMOS OTA as shown in figure 4. An essential component of the proposed BICS is the current mirror circuit which has property that, the reference current in one branch of the circuit is accurately reproduced in the other branch, in a constant current stage. BICS's ability to detect abnormal current due to physical defects depends on performance of current mirror. When the BICS is in test mode, the constant reference current is set to approximately the same value as the quiescent state current. The advantage of proposed BICS is that it does not require any external voltage or current source [16, 17].

The CUT works in two modes: the normal mode and the test mode. The BICS is totally isolated from the CUT in the normal mode so that the operation of CUT is not affected by the BICS whereas in the test mode, the CUT is connected to the BICS and it first compares a quiescent state current consumed by the CUT with a reference current. The output signal PASS/FAIL is set to 1, when the quiescent state current is greater than the reference current, which indicates the existence of fault in the circuit. The output signal PASS/FAIL is set to 0, when the quiescent state current is less than the reference current, which indicates the nonexistence of fault [18,19].The built-in current sensor of the present work requires less area and is more efficient than the conventional current sensors. It is observed that with the use of a novel fault injection technique, combined with a BICS design, has significantly improved the testing of analog and mixed signal integrated circuits.

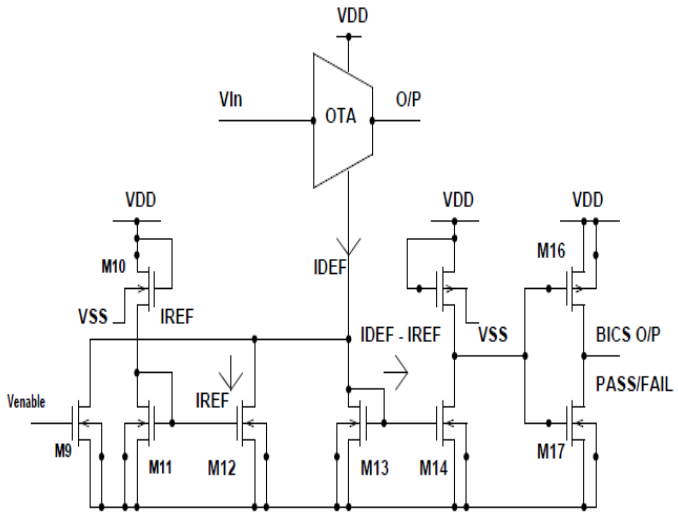


Fig. 4: CUT with CMOS Build-in–current (BICS) sensor

VI. **Analog Fault Modelling**

Catastrophic (hard) and parametric (soft) faults are the types of faults which occur in analog or mixed-signal integrated circuit. Catastrophic faults (hard faults) are the faults which are due to random defects causing failure in various elements of the circuit. These catastrophic faults include short, open or large variation in design parameter causes complete failure of the circuit. Parametric (soft) faults are faults due to statistical fluctuation in the manufacturing process, resulting small deviation of CUT parameters from its tolerance band [20, 21]. The faults considered in this study comprise catastrophic faults which include seven open and fifteen bridging faults. An open fault and short fault are simulated by introducing high resistance of 100 MΩ in series and low resistance of 10Ω in parallel respectively.

VII. **Simulation Results and Tables**

The fault coverage is achieved by the combined test approach based on the simulated results obtained from PSPICE (Cadence PSPICE A/D Simulator) simulations. SPICE level 7 MOS model parameters are used in simulation using 0.18µm n-well CMOS technology.

The testable CMOS OTA in fig.1 is simulated for verification of the proposed OBT and I_{DDQ} testing. The transient analysis for a sinusoidal input of 5mV peak-to-peak at 50 KHz applied to the non inverting terminal of CUT is shown in figure 5. At the output of the CUT, non-inverted waveform of 1.6V peak-to-peak is obtained, giving voltage gain of 100 at 50 KHz.

ISSN:2277-1581
01 October 2016

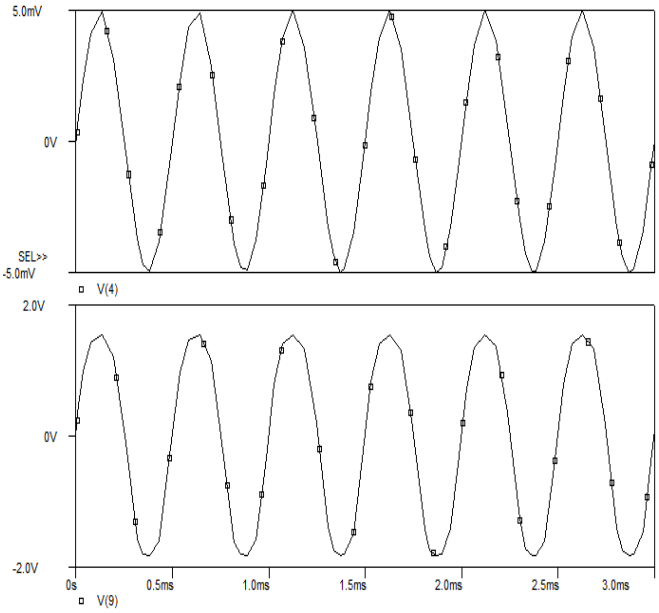
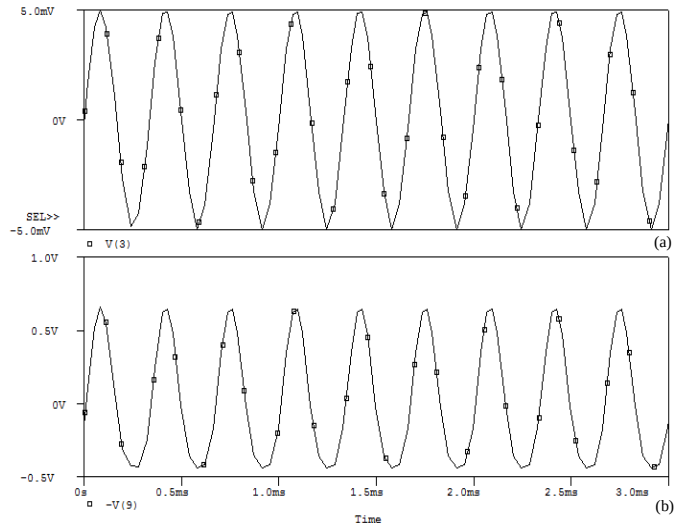


Fig. 5: Simulated input and output of CUT

A. OBT Simulation Results

CUT is converted into to an oscillator using quite simple feedback circuit as shown in figure 2 which has nominal oscillation frequency of 755KHZ. Figure.6 shows time domain oscillation response of CUT, time domain oscillation response of the CUT as an oscillator and the frequency response of the circuit under test. The fault-free oscillation frequency observed to be 752KHZ which was slightly shifted from the cut-off frequency of the circuit [18], [19]. Monte Carlo simulation is performed to determine the undetectable tolerance band for the frequency. The tolerance of 15% and 10% has been considered for capacitances C1, Cc and resistances R1, R2 respectively for the oscillator circuit. The Fast Fourier Transform (FFT) of the output signal shows that the oscillation signal has lower and upper frequency deviation bounds of -4.25% and +5.05% respectively.



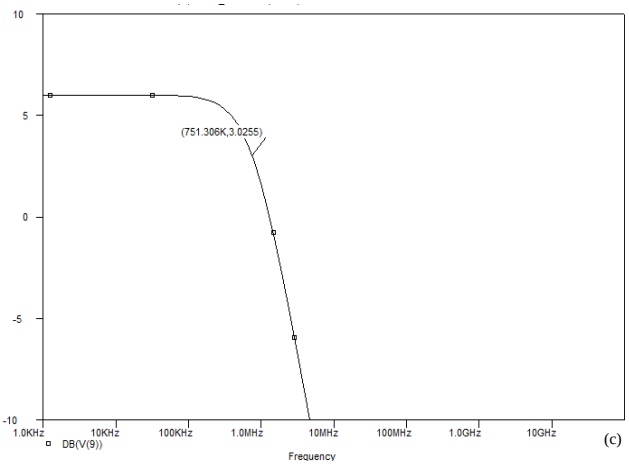


Fig. 6: (a) Output frequency of CUT (b) Oscillation frequency of CUT as an oscillation (c) Cut-off frequency of CUT

The faults which produced oscillation frequency deviation outside this tolerance band were considered detectable. It is observed that the seventeen faults out of twenty three fault deviate from nominal oscillation frequency range whereas four faults resulted in loss of oscillation, thus twenty one faults have been detected with fault coverage of 91%. The results also show that two faults could not be detected, since the deviation observed in oscillation frequency with respect to nominal frequency was within the tolerance limit. Tables 1 present the effects of the injected faults on the oscillation frequencies and percentage deviations from the fault-free frequency.

Table 1. Injected Faults in the CUT

Component	$\Delta C/C$	$\Delta f_{osc}/f_{osc}$	$\Delta C/C$	$\Delta f_{osc}/f_{osc}$	$\Delta C/C$	$\Delta f_{osc}/f_{osc}$
M1	GDS	20%	DSS	-9.93%	OPEN	NO
M2	GDS	-10%	DSS	-9.3%	OPEN	-6.91%
M3	GDS	3%	DSS	-25%	OPEN	35.77%
M4	GDS	NO	DSS	2%	OPEN	180%
M5	GDS	32.18%	DSS	6.38%	OPEN	23%
M6	GDS	-30.55%	DSS	-10.3%	OPEN	NO
M7	GDS	6.38%	DSS	NO	OPEN	110%
C_C	SSF	12.5%	-	-	OPEN	-10.39%

ΔC / C: Percentage of the faults injected into component $\Delta fosc$ / fosc: Variation of the oscillation frequency from its nominal value, NO: No oscillation, GDS: Gate – Drain Short, DSS: Drain - Source Short, SSF: Struck Short Fault.

Table 2 summarizes the fault coverage obtained by oscillation testing in terms of short and open faults injected. It

ISSN:2277-1581
01 October 2016

can be seen from the table 2 that the overall fault coverage obtained for all faults injected is 91%.

Table 2. Fault Coverage of Oscillation Based Testing

Fault Type	Total Faults Injected	Fault Detected (with Oscillation)	Fault Detected (without Oscillation)	Fault Undetected (with Oscillation)	Fault Coverage
Short	15	11	2	2	73.3%
Open	8	6	2	0	100%
Total	23	17	4	2	91.3%

B. I_{DDQ} Simulation Results

The proposed BICS is simulated using 0.18um technology using PSPICE. The simulated result of two stage OTA without BICS is shown in figure 5 whereas figure 7 shows the simulated output response of CUT with BISC when fault are not activated i.e. when CUT is in normal mode. It is observed that degradation in the voltage level due to presence of the BICS is order of 20mV which can be considered negligible compared to the supply voltage. Therefore there is no performance degradation of the circuit under test due to the presence of proposed BICS. IREF is set to 400µA.

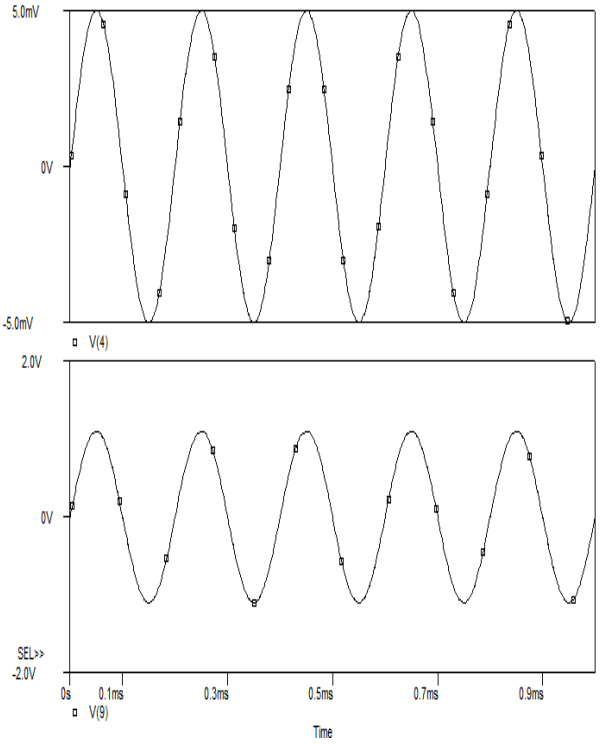


Fig. 7: Simulated input and output response of CUT with BICS enable without fault

Total twenty three faults introduced which includes fifteen short faults and eight open faults as shown in Table 3.

Table 3. Simulated I_{DDQ} (I_{REF} = 400µA)

Component	Fault Type	Simulated I_{DDQ}	Fault Type	Simulated I_{DDQ}	Fault Type	Simulated I_{DDQ}
M1	GDS	500 µA	DSS	750 µA	OPEN	990 µA
M2	GDS	1000 µA	DSS	450 µA	OPEN	650 µA
M3	GDS	980 µA	DSS	870 µA	OPEN	1100 µA
M4	GDS	990 µA	DSS	1000 µA	OPEN	800 µA
M5	GDS	570 µA	DSS	910 µA	OPEN	150 µA
M6	GDS	600 µA	DSS	890 µA	OPEN	1800 µA
M7	GDS	690 µA	DSS	550 µA	OPEN	200 µA
C_C	SSF	1000 µA	-	-	OPEN	730 µA

GDS: Gate – Drain Short, DSS: Drain - Source Short, SSF: Struck Short Fault

It is observed all the short faults and six out of eight open faults have been detected by I_{DDQ} technique. The overall fault coverage by using this technique is 91.3% as summarized in Table 4.

Table 4. Simulated Fault Coverage by I_{DDQ} Testing

Fault Type	Total Faults	Fault Detected	Fault Undetected	Fault Coverage
Short	15	15	0	100%
Open	8	6	2	75%
Total	23	21	2	91.3%

The faults which are detected by OBT with loss of oscillation and undetected by OBT are detected by I_{DDQ} method which results in fault confirmation. The simulation results showed that all the twenty three faults are detected by combined oscillation and I_{DDQ} testing technique which provides 100% fault coverage.

VIII. Conclusion

In this paper, combined oscillation based I_{DDQ} testing technique has been explored on operational transconductance amplifier using 0.18um n-well CMOS technology using PSPICE. The proposed testing is an effective technique for improving the quality and reliability of analog and mixed integrated circuits. It provides 100% fault coverage with low

area overhead and small test time. Thus, combined oscillation and I_{DDQ} testing methodology is a valuable tool to achieve high fault coverage and also improve reliability and quality of analog and mixed- signal CMOS integrated circuits without incurring significant test development cost.

References

i. *Linda S. Milor, "A Tutorial Introduction to Research on Analog and Mixed-Signal Circuit Testing", IEEE Transactions on circuits and system-II: Analog and digital Signal processing, Vol. 45, No.10, pp. 1389-1407, 1998.*

ii. *Michael L. Bushnell and Vishwani D Aggarwal, "Essentials of Electronic Testing for Digital, Memory and Mixed–Signal VLSI circuit", Kluwer Academic Publication.*

iii. *G. Huertas, D. Vazquez, E.J. Peralias, A. Rueda, J. L. Huertas, " Practical Oscillation-Based Test of Integrated Filters", IEEE Design & Test of Computers, Vol. 1, No.6, pp. 64-72, 2002.*

iv. *Peter Mark, Anton Biasizzo and Franc Novak, "Measurement of Accuracy of Oscillation-Based Test of Analog-to-Digital Converters", ETRI Journal, Vol. 32, No.1, 2010.*

v. *K. Arabi and B. Kaminski, "Design for Testability of Embedded Integrated Operational Amplifiers", IEEE Solid-State Circuit, Vol. 33, pp. 573-58, 1998.*

vi. *R Rajsuman, "I_{DDQ} testing for CMOS VLSI", Proceeding of IEEE, Vol. 8, Issue 4, pp. 544-566, 2000.*

vii. *Bhavesh H.Soni, Rasika N Dhavse, "Design of OTA using 0.35µm Technology", International Journal of Wisdom Based computing, Vol.1, 2011.*

viii. *Bijay K Sharma, "Oscillation Based Test Method of Parameterization of Open Op Amp and its Authentication", AEU-International Journal of Electronics and Communication, Vol. 68, Issue 7, pp 595-60, 20141.*

ix. *Sankari M.S and P. Sathish Kumar, "Oscillation Test methodology of Built- In Analog Circuits", IJCER, Vol. 2, No. 3, pp. 868-877, 2012.*

x. *Miona Andrejevic Stosovic, Miljana Milic and Vanco Litovski, "Analog filter diagnosis using the Oscillation Based Method", Journal of Electrical Engineering, Vol. 63, No.6, pp. 349-356, 2012.*

xi. *Masood-ul-Hasan, Yichuang Sun, Xi Zhu and James Moritz, "Osillation-based DFT for second order OTA-C filter", IEEE Symposium on Circuits and Systems, pp. 720-723, 2008.*

xii. *K. Arabi and B. Kaminska, "Testing Analog and Mixed-Signal Integrated Circuits using Oscillation-Test Method", IEEE. Trans. on Computer-Aided Design of Integrated Circuits and Systems, Vol. 16, Issue 7, pp. 745-753, 1997.*

xiii. *Raja Sen, Arko Banerjee, Satyaki Banerjee, Sayanta Roychowdhury, "Design of an oscillator using CMOS operational transconductance amplifier", International Journal of electrical and computing engineering, Vol. 1, Issue 1, pp.23-29, 2014.*

xiv. *S Matakias, Yiorgos, A Arapoyanni, and T Haniotakis, "A current monitoring technique for I_{DDQ} testing in Digital integrated circuits Integration", The VLSI journal, Vol. 50, 2015, pp. 48-60, 2015.*

xv. *S Matakias, Y Tsiatouhas, A Aprapovanni, TH Haniotakis, G Prenat, and S Mir, "A Built –In I_{DDQ} Testing circuit", Proceeding of ESSCIRC, Grenoble, France, pp. 471-474, 2005.*

xvi. *T L Shen, J C Daly and J C Lo, "On Chip current sensing circuit for CMOS VLSI", Proc. IEEE VLSI Test Symposium, paper 16, 1992.*

xvii. *M W T Wong, A M F Yu, C K Li., "Application of I_{DDQ} test in failure analysis of micro-controller devices", Microelectronic Journal, Vol. 32, pp. 29-34, 2001.*

xviii. *M. L. Ali and N.H Khamis, "Design of a current sensor for I_{DDQ} testing of CMOS IC", American Journal of applied Sciences 2, pp. 682-687, 2005.*

xix. *Ekekon, S Maltabas and M Margala,"Novel programmable built in current sensor for analog, digital and mixed signal circuits" proceeding of IEEE International Symposium on Circuits and Systems (ISCAS), pp. 3545-3548,2010.*

xx. *Karim Arabi and Bozena Kaminski, "Parametric and Catastrophic Fault coverage of Analog Circuits in Oscillation-Test Methodology", Proceeding of 15th IEEE VLSI Test Symposium, pp.166-171, 1997.*

xxi. *I Masahiro, D S Ha, T Yamaguchi, Y Hashimoto and T Ohmi, "IDDT testing: An Efficient Method for Detecting Delay Faults and Open Defects", IEEE International workshop on Defect based Testing, Los Angeles, CA, USA, 2001, pp. 23-28, 2001.*

xxii. *P Engelke, I Polian, M Renovell and B Becker, "Simulating resistive bridging and stuck-at fault", International Test conference, pp. 1051-1059, 2003.*